FLASH MEMORY WITH RDRAM INTERFACE

FIELD OF THE INVENTION

[01] The present invention relates generally to memory devices and in particular the present invention relates to a non-volatile flash memory interface.

BACKGROUND OF THE INVENTION

[02] A typical Flash memory comprises a memory array that includes a large number of memory cells arranged in row and column fashion. Each of the memory cells includes a floating gate field-effect transistor capable of holding a charge. The cells are usually grouped into blocks. Each of the cells within a block can be electrically programmed in a random basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation. The data in a cell is determined by the presence or absence of the charge in the floating gate.

[03] A synchronous DRAM (SDRAM) is a type of DRAM that can run at much higher clock speeds than conventional DRAM memory. SDRAM synchronizes itself with a CPU's bus and is capable of running at 100 MHZ, about three times faster than conventional FPM (Fast Page Mode) RAM, and about twice as fast EDO (Extended Data Output) DRAM and BEDO (Burst Extended Data Output) DRAM. SDRAM's can be accessed quickly, but are volatile. Many computer systems are designed to operate using SDRAM, but would benefit from non-volatile memory.

[04] Advances in DRAM interfaces has resulted in double data rate (DDR) DRAMs. These memory devices provide data communication that is synchronized to both rising and falling edges of a clock signal. While DDR DRAMs provide for fast data communications, the data is stored in a volatile manner. Likewise, Rambus memory devices, such as RDRAM, provide a packet based alternative high-speed

memory choice. The RDRAM provides similar operations as the DDR DRAM, and is volatile in nature.

[05] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a non-volatile memory that can communicate at fast DRAM speeds.

SUMMARY OF THE INVENTION

[06] The above-mentioned problems with non-volatile memories and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[07] In one embodiment, a flash memory comprises an array of non-volatile memory cells, data connections, an interconnect configuration compatible with a rambus dynamic random access memory (RDRAM), and output circuitry to provide output data on the data connections on rising and falling edges of a clock signal.

[08] In another embodiment, a flash memory comprises an array of non-volatile memory cells, data connections, a clock signal connection to receive a clock signal, and an interconnect configuration compatible with a rambus dynamic random access memory (RDRAM). Output circuitry provides output data on the data connections on rising and falling edges of the clock signal, and input circuitry receives input data on the data connections on rising and falling edges of the clock signal.

[09] A method of reading a flash memory comprises providing a read command, providing memory cell addresses, reading first and second data words from non-volatile memory cells, outputting the first data word on a rising edge of a clock signal following a rambus dynamic random access memory (RDRAM) compatible format, and outputting the second data word on the falling edge of the clock signal following the rambus dynamic random access memory (RDRAM) compatible format.

[10] In yet another embodiment, a flash memory comprises an array of non-volatile memory cells having bit lines couplable to the non-volatile memory cells, sense amplifier circuitry coupled to the bit lines to detect a differential voltage between the bit lines, and pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell. The memory includes data connections, a clock signal connection to receive a clock signal, and has an interconnect configuration compatible with a rambus dynamic random access memory (RDRAM). Output circuitry provides output data on the data connection on rising and falling edges of the clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[11] Figure 1 is a block diagram of a non-volatile memory of one embodiment of the present invention; and

[12] Figure 2 illustrates an interconnect pin assignment of one embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[13] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

[14] The present invention provides a non-volatile memory device that is compatible with rambus dynamic random access memory (RDRAM). RDRAMs generally provide output data that is synchronized to both transitions of a clock signal.

[15] Referring to Figure 1, a block diagram of a flash memory according to one embodiment of the present invention is described. The memory device includes an array of non-volatile floating gate memory cells. As known to those in the art, the non-volatile memory cells store a charge on the floating gate. The floating gate charge changes the threshold voltage of the memory cell. In traditional flash memory cells, a current-sensing scheme was employed to read the memory cells. The present invention uses a voltage-sensing scheme to read the non-volatile memory cells Possible voltage-sensing schemes are described in U.S. Patent Applications "Differential Sensing in a Memory Using Two Cycle Pre-Charge" Serial No. 09/648,706, filed 8/25/00; "Bit Line Pre-Charge in a Memory" Serial No. 09/648,701, filed 8/25/00; "Adjustable Pre-Charge in a Memory" Serial No. 09/648,722, filed 8/25/00; and "Differential Sensing in a Memory" Serial No. 09/648,723, filed 08/25/00, each incorporated herein by reference.

[16] The flash memory of the present invention can be arranged in numerous different architectures, and Figure 1 is merely a representative architecture of the present invention. Memory device 100 includes an array of non-volatile flash memory cells 102 arranged in a plurality of addressable banks. Each memory bank can contain addressable sectors of memory cells. The data stored in the memory can be accessed using externally provided location address packets received by de-multiplex circuits 104 and 106. The address packets are decoded using column and row decode circuitry 108 and 110.

[17] Write buffer 112 and de-multiplex circuit 114 are provided to write data received on DQ lines. Similarly, multiplex circuit 116 provides read data on the DQ lines. Sense amplifier circuitry 120 is used to read the data from the flash cells, and I/O gating 122 is used to communicate with the array. Sense amplifier circuitry 120 includes bit line precharge circuitry used to read the non-volatile memory cells.

Command logic 124 is provided to control the basic operations of the memory device. The command logic also includes control registers used to store data for memory operation control. Other embodiments can include separate the read and write paths to provide for the power requirements of writing to the flash cells.

[18] Figure 2 illustrates an interconnect pin assignment of one embodiment of the present invention. The memory package 150 has an interconnect configuration that is substantially similar to available RDRAM packages. Although the present invention shares interconnect labels that are appear the same as RDRAM's, the function of the signals provided on the interconnects are described herein and should not be equated to RDRAM's unless set forth herein.

[19] The flash memory provides an RDRAM interface that provides two data words per clock cycle. Read accesses to the memory can be burst oriented. That is, memory accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

[20] The present invention uses a data-sensing scheme that increases the speed of read operations and reduces current consumption compared to conventional flash memory devices. That is, conventional flash memories use a current sensing technique that compares a current conducted by a memory cell to a reference current. This sensing technique is slower than a DRAM differential voltage-sensing scheme. Further, to read numerous columns of memory cells simultaneously, conventional current sensing techniques consume a relatively large current.

[21] An embodiment of the present invention uses a voltage sensing technique to read the non-volatile memory cells. In one embodiment, differential digit lines are pre-charged to different voltage levels prior to accessing a memory cell. For example, an active digit line that is coupled to a read memory cell can be pre-charged to a voltage that is greater than a complementary digit line. If the read memory cell is un-programmed (conducts current when read), the active digit line is quickly discharged

below the complementary digit line voltage. If the read memory cell is programmed (does not conduct current when read), the active digit line voltage remains above the complementary digit line voltage. A differential voltage sensing circuit can be used to detect and amplify the digit line voltages. Further, pre-charging the digit lines to a differential level is not limited to a specific technique, but can be accomplished using charge sharing, a bias circuit or the like.

[22] The present invention allows both volatile and non-volatile memory devices to use a unified communication bus. As such, a separate non-volatile bus is eliminated. Both non-volatile and volatile memories use the volatile memory bus. Further, both memories respond to common command signals, although the command signals may be interpreted differently by the memories.

CONCLUSION

[23] A flash memory has been described that has an interface corresponding to a rambus dynamic random access memory (RDRAM). The memory samples commands and addresses on a rising edge of a clock signal. The read and write data are provided on both the rising edge and the falling edge of the clock signal.

[24] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.